Lesson 6

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Identifying Purposes and Characteristics of Memory

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Introduction

- Memory often is called RAM, for random access memory. Main memory is called RAM because you can randomly (as opposed to sequentially) access any location **directly** in memory.
- RAM is the place in a computer where the operating system, application programs, and data in current use are kept so that they can be quickly reached by the computer's processor.
- RAM is much faster to read from and write to than the other kinds of storage in a computer, the hard disk, floppy disk, and CD-ROM. However, the data in RAM stays there only as long as your computer is running.
- When you turn the computer off, RAM loses its data. When you turn your computer on again, your operating system and other files are once again loaded into RAM, usually from your hard disk.

- memory upgrades tend to afford the greatest performance increase
- Microsoft always says “Add More Ram”
- Motherboards have memory limits
  Operating systems have memory limits
  CPUs have memory limits.
- most motherboard manufacturers document the quantity and types of modules that their equipment supports.
- Don’t be surprised when you attempt to install a single module of the highest available capacity in your motherboard, and the system doesn’t recognize the module,

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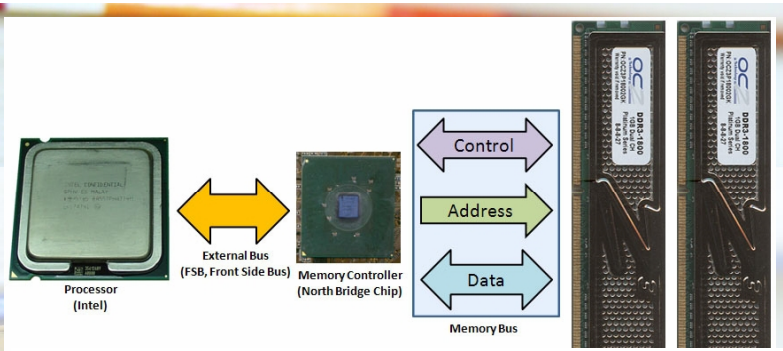
Location of memory within a system

Memory Controller vs. Bus Cycle

- Memory Controller is placed between **RAM** and **CPU** which
  - handles the movement of data to and from the CPU and the system memory banks.
  - responsible for the integrity of the data as it is swapped in and out
- This circuit is physically inside the chipset (north bridge)
- Bus cycle :are Each transaction between the CPU and memory



The wires from the data bus will carry **data** that is being read (i.e. transferred from the memory to the memory controller and then to the CPU) or written (i.e. transferred from the memory controller to the memory, coming from the CPU).

The wires from the **address** bus tells the memory modules where exactly (i.e. which address) that data must be retrieved from or stored.

And the **control** wires send commands to the memory modules, telling them what kind of operation is being done – for example, if it is a write (store) or a read operation.

There are two primary methods of ensuring that the data received is the same as the data sent:

1. parity
2. error-correction coding (ECC).

1- Parity checking

- *Parity checking is used to detect memory corruption between the time that data is written to memory and the time that it is read back*
- *Parity checking* is a old error-checking scheme that offers no error correction.
- **is a method of ensuring data integrity that adds an extra bit (the parity bit) along with each 8-bit bus cycle.**
- Parity checking works most often on a byte, or 8 bits, of data. A ninth bit is added at the transmitting end and removed at the receiving end so that it does not affect the actual data tra

Module Type	Bit Width of Non-Parity SIMM	Bit Width of Parity SIMM
30-Pin SIMM	8 bits	9 bits
72-Pin SIMM	32 bits	36 bits
168-Pin DIMM	64 bits	72 bits

The four most common parity schemes affecting this extra bit are known as

– Even
– odd,
– Mark
– and space.

Even parity

- *In Step 1*, set the value of the parity bit based on the even number that represents the sum of the data bits as the
- first step.

1	1	1	0	1	0	1	1	

num of 1 is (6) is even so parity =0

1	1	1	0	1	0	0	1	

num of 1 is (5) is odd so will add have 1 in parity to make the total number of 1 is even

- *In Step 2*, the string goes into DRAM.
- *In Step 3,* When the data is read back from memory, the parity circuit this time acts as a checker.. If the parity bit matches the data is passed on.
- If it fails the test, an error is reported. (difrent from operating system.)

Odd parity

- *In Step 1*, set the value of the parity bit based on the odd number that represents the sum of the data bits as the
- first step.

1	1	1	0	1	0	1	1	

num of 1 is (6) is even so parity =1

1	1	1	0	1	0	0	1	

num of 1 is (5) is odd so will add have 0 in parity to make the total number of 1 is odd

- *In Step 2*, the string goes into DRAM.
- *In Step 3,* When the data is read back from memory, the parity circuit this time acts as a checker.. If the parity bit matches the data is passed on.
- If it fails the test, an error is reported.

Mark and space parity

- Mark and space parity are used in systems that want to see 9 bits for every byte transmitted but don't compute the parity bit's value based on the bits in the byte.
- Mark parity always uses a 1 in the parity bit,

- space parity always uses a 0.

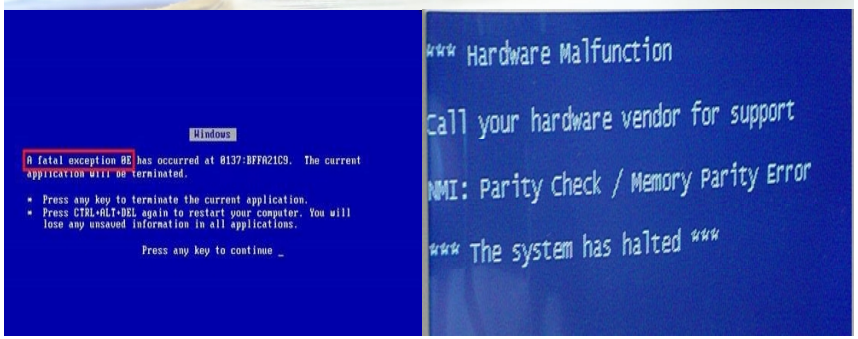
- These schemes offer less error detection capability than the even and odd schemes because only changes in the parity bit can be

How parity works

- When the CPU requests data from memory, the data byte is retrieved along with the parity bit that was generated when the byte of information was stored in memory.
- The system looks at the data byte and calculates whether the parity bit stored in memory should be set to 1 or 0.
- It then compares the answer it has just generated with the value of the parity bit stored in memory.
- If the two match, the integrity of the information in memory is considered okay, the parity bit is stripped from the data byte, and the data is delivered to the CPU.
- If the two differ, you have a parity error, meaning that there is a problem with the integrity of the data stored in memory.

parity error

- which is usually used to instruct the processor to immediately halt.
- This is done to ensure that the incorrect memory does not end up corrupting anything.



Parity problem

- The problem of Parity that cant detect multiple bit error
- It can only detect single bit error
- No error correction

2- Error Checking and Correction

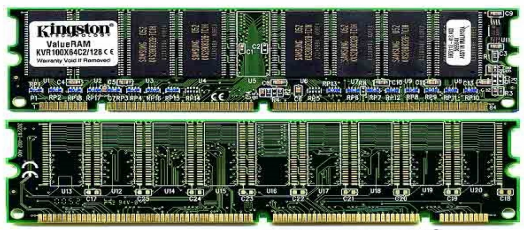
- If memory supports ECC, check bits are generated and stored with the data.
- An algorithm is performed on the data and its check bits whenever the memory is accessed.
- If the result of the algorithm is all zeros, then the data is deemed valid and processing continues.
- ECC can detect single- and double-bit errors and actually correct single-bit errors.
- If the date is not valid in the 2 cases it will ask the processor to send the data again

Important Memory Terms

- Single- and double-sided memory
- Single- and dual-channel memory

Single- and double-sided memory

- These terms have nothing to do with the physical attachment of chips to the modules.
- *Double-sided memory is essentially treated by the system as **two separate memory*** modules.
- Motherboards that support such memory have memory controllers that must switch between the two "sides" of the modules and, at any particular moment, can only access the side they have switched to.
- Double-sided memory allows more memory to be inserted into a computer using half the physical space of *single-sided memory, which requires no switching by the memory controller.*

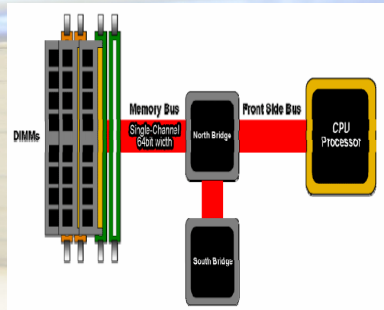


- One common point of confusion, not related to capacity, when installing memory includes lack of recognition of four modules, when two or three modules work fine,
- for example. In such a case, let's say your motherboard's memory controller supports a total of four modules.
- Recall that a double-sided module acts like two separate modules.
- If you are using double-sided memory, your motherboard might limit you to two such modules, comprising four sides (essentially four virtual modules), even though you have four slots on the board.
- If instead you start with three single-sided modules, when you attempt to install a double-sided module in the fourth slot, you are essentially asking the motherboard to accept five modules, which it cannot.

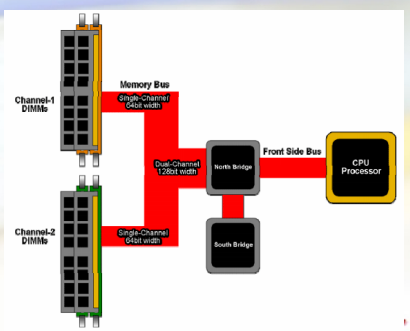
Single- and dual-channel memory

Dual Channel DDR structure uses Twin Bank mode, and requires two memory modules plugged into the appointed DIMM slots in order to enable 2 Channel DDR.

There is no such thing as Dual Channel DDR Memory Modules. Regular DDR is installed two modules at a time, each module controlled by a separate channel of the memory controller.



▲ Simplified Single-Channel memory operating at a total of 64-bit



▲ Simplified Dual-Channel memory operating at a total of 128-bit

- **In order to enable dual channel technology you need to have:**
- Compatible chipset and motherboard (Intel CPU) or compatible CPU (AMD).
- Two or four identical memory modules, compatible with the technology supported by the motherboard (DDR-SDRAM, DDR2-SDRAM or DDR3-SDRAM).
- speeds, capacities, or numbers of sides)
- Note :dual-channel is technology on which the motherboard is based, not ram

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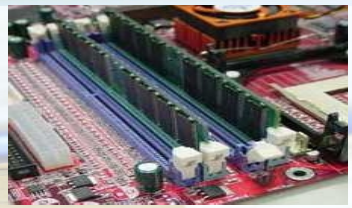
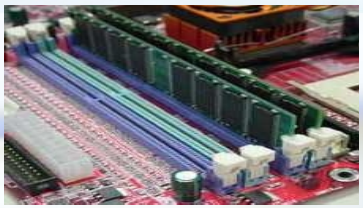
Single Channel vs.. Dual Channel





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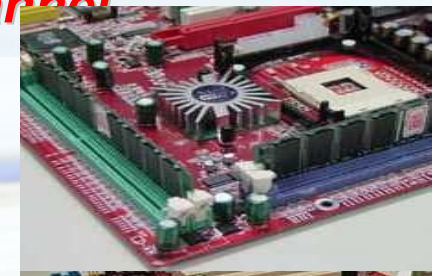
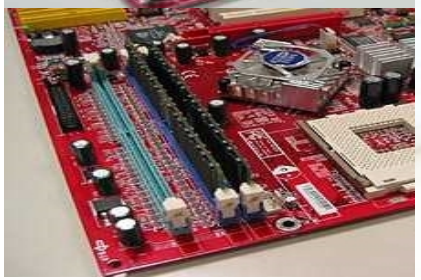
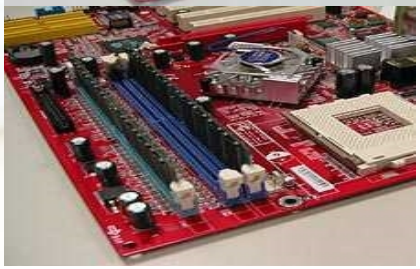
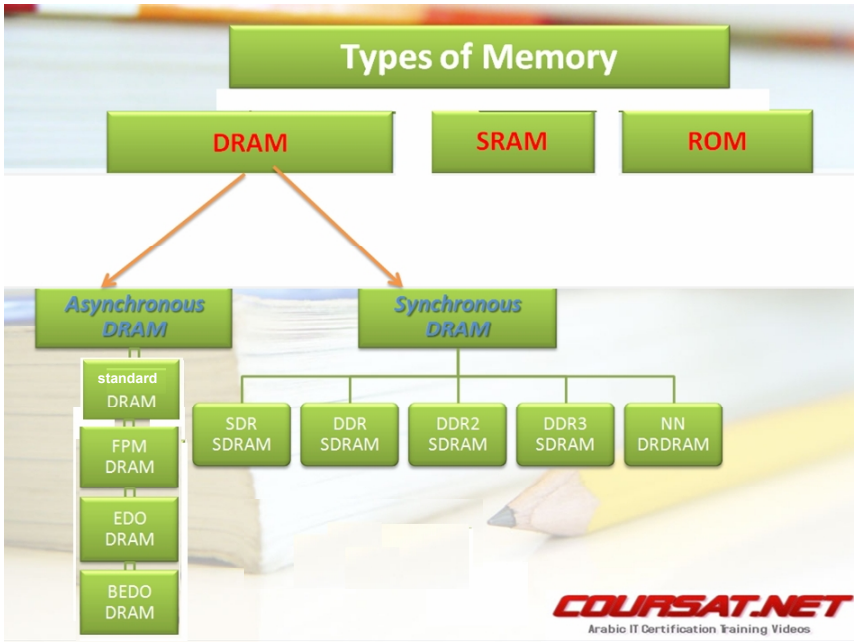
Single Channel vs.. Dual Channel









YEAR INTRODUCED	TECHNOLOGY	SPEED LIMIT
1987	FPM	50ns
1995	EDO	50ns
1997	PC66 SDRAM	66MHz
1998	PC100 SDRAM	100MHz
1999	RDRAM	800MHz
1999/2000	PC133 SRAM	133MHz (VCM option)
2000	DDR SDRAM	266MHz
2001	DDR SDRAM	333MHz
2002	DDR SDRAM	434MHz
2003	DDR SDRAM	500MHz
2004	DDR2 SDRAM	533MHz
2005	DDR2 SDRAM	800MHz
2006	DDR2 SDRAM	667 - 800MHz
2007	DDR3 SDRAM	1066 - 1333MHz

1-Dynamic RAM(DRAM)

- Dynamic RAM gets its name from the fact that the information stored in DRAM needs to be constantly refreshed.
- Refreshing involves reading the bits of data stored in DRAM and then rewriting the same information back.

2-Static RAM (SRAM)

- **Static RAM (SRAM)**
- The chips are more complex Faster but more costly than DRAM "30X in price and size"
- Used for cache memory in systems "L1,L2,L3"
- SRAM does not use capacitors to store 1s and 0s.
- Instead, SRAM uses a special circuit called a *flip-flop* it does not. be refreshed because it uses the flip-flop circuit to store each bit.

- **Dynamic RAM (DRAM).**
- Slower but Cheap enough to make it possible to use it in large quantities in PC systems.
- DRAM use capacitors to store 1s and 0s must be continually refreshed to make sure the data is held.

3-Read-Only Memory (ROM)

- *is a type of memory that you cannot write to.*
- Information is written to ROM chips by the manufacturer, and this information cannot be changed.
- One of the major uses for ROM is storing the system *BIOS (Basic Input-Output System), which contains Power-On Self-Test (POST) routines*

1-Programmable ROM (PROM),

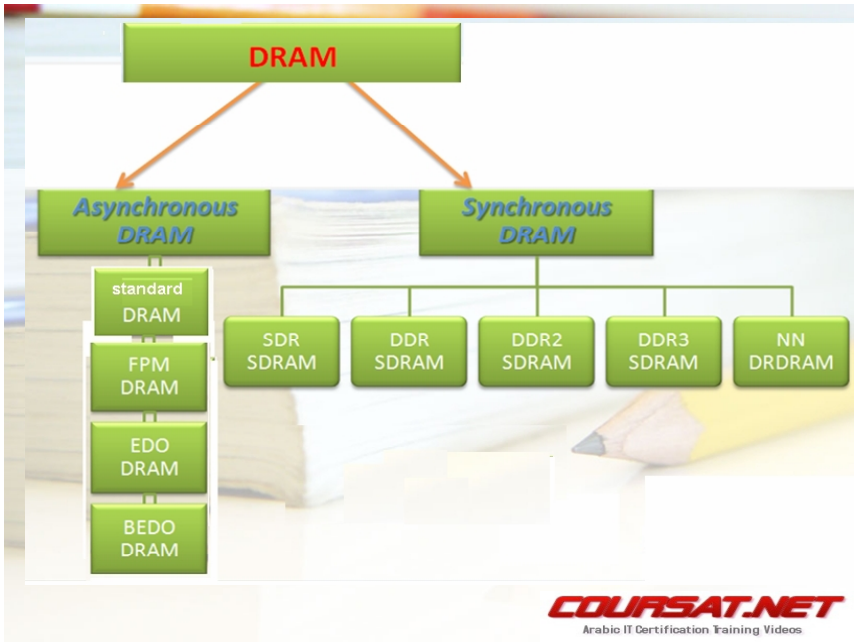
which could be written to for the first time in the field using a special programming device but then no more.

2-Erasable PROM (EPROM),

which was able to be erased using ultraviolet light and subsequently reprogrammed using the original programming device.

3-Electrically Erasable PROM (EEPROM) Flash Rom

The manufacturer writes the software instructions into the ROM chip, but you can update these instructions by running a special software setup program provided by the manufacturer. Download it from manufacturer Web site.



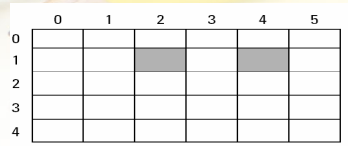
Asynchronous DRAM

- Asynchronous DRAM *is characterized by its independence from the CPU's external* clock.
- Asynchronous DRAM chips have codes on them that end in a numerical value that is related to (often one tenth of the actual value) the access time of the memory.
- **Access Time** is the amount of time it takes for the RAM to provide requested data to the memory controller. denoted in nanoseconds (ns) Here, smaller is better
- The access speed of a chip is usually printed on the chip (often as part of the identification number).
- Common access times attributed to asynchronous DRAM were in the 40- to 120-nanosecond (ns) vicinity.

If the CPU wanted some data from RAM, the Northbridge sent the necessary signals to the DRAM, waited a certain number of clock ticks, and then accessed the RAM again to get the data. The number of clicks was not exact, but rather rounded up to ensure that the Northbridge wouldn't access DRAM before the necessary data was ready. This rounding up wasted system time, but FPM and EDO DRAM was too

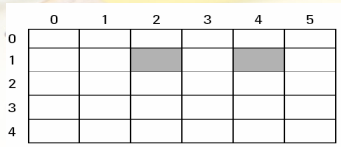
1-Standard DRAM

- With *standard DRAM, the CPU requests data* by sending the address of the row and the address of the column for every block of data that needs to be read to the memory controller.
- The memory controller then fetches the information from that memory location.



2- Fast Page-Mode RAM (FPM)

- 1990s
- It offered a 25-MHz clock rate and a maximum bandwidth of 200 Mbps.
- It was faster because the methods it used for locating data within RAM was the faster .
- *Fast Page Mode (FPM) improves the performance of standard DRAM by not* requiring a row address for each request to memory, assuming that the next block of data is on the same row (which in most cases will be true).



3- Extended Data Out RAM (EDO)

- Introduced in 1994, (EDO) RAM supported a clock rate of 40 MHz and a maximum bandwidth of 320 Mbps.
- EDO RAM yields a 10 to 15 percent performance improvement by eliminating the 10-nanosecond delay incurred by waiting for the memory controller to issue the next memory address. (it allows one access to begin as another one finished)
- So similar are FPM and EDO RAM that a system that does not support EDO RAM can usually use EDO memory modules anyway, though there is no performance improvement.

4-Burst Extended Data Output DRAM (BEDO DRAM)

- *is a bursting-type technology.*
- *The word burst refers to the fact that when one memory address is requested and that* address is retrieved, the system bursts into the next couple of blocks and reads those as well.
- The theory behind BEDO is that the system has already gone through the trouble of locating that block, and chances are that the next request will be for the next block, so why not take that information while the memory controller is already there? If that extra block is the next requested block from the CPU, the memory controller already has the data and can pass it to the CPU immediately.
- BEDO is 50 percent faster than EDO.
- It works well with microprocessors that operate up to 66 MHz

Synchronous DRAM

- *Synchronous DRAM (SDRAM) shares a common clock signal with the computer's system-* bus clock,
- This characteristic ties SDRAM to the speed of the FSB and, hence, the processor, eliminating the need to configure the CPU to wait for the memory to catch up.
- The speed of SDRAM is rated in MHz rather than in nanoseconds (ns).

1-Single data rate SDRAM (SDR SDRAM)

- SDRAM is tied to the system clock and is designed to be able to read or write from memory at 1 clock cycle per access at memory bus speeds up to 100 MHz or even higher.
- every time the system clock ticks, one bit of data can be transmitted per data pin, limiting the bit rate per pin of SDRAM to the corresponding numerical value of the clock's frequency.

Stander name	Module name	FSB Speed	Memory bus (64 bit)	Module Throughput
PC66	PC66	66 MHz	8 bytes	**528 MBps**
PC100	PC100	100 MHz	8 bytes	**800 MBps**
PC133	PC133	133 MHz	8 bytes	**1067MBps**
Module Throughput =FSB Speed (MHz)X Memory bus(bytes)				

Double data rate (DDR) SDRAM

- It achieves nearly twice the bandwidth of the preceding single data rate (SDR) SDRAM by double pumping (transferring data on the rising and falling edges of the clock signal) without increasing the clock frequency.

Stander name (Chips name)	Module name	Actual FSB Speed	Advertised FSB Speed (2x) Data Rate	Memory bus (64 bit)	Module Throughput (MBps)
DDR-200	PC-1600	100	200	8 bytes	**1600 MBps**
DDR-266	PC-2100	133	266	8 bytes	**2100 MBps**
DDR-300	PC-2400	150	300	8 bytes	2400 **MBps**
DDR-333	PC-2700(2667)	166	333	8 bytes	**2700 MBps**
DDR-366	PC-3000	183	366	8 bytes	3000 **MBps**
DDR-400	PC-3200	200	400	8 bytes	**3200 MBps**
DDR-433	PC-3500	216	433	8 bytes	3500 **MBps**
DDR-466	PC-3700	233	466	8 bytes	3700 **MBps**
DDR-500	PC-4000	250	500	8 bytes	4000 **MBps**
DDR-533	PC-4300	266	533	8 bytes	4300 **MBps**
Module Throughput =FSB Speed (MHz) X Memory bus (bytes)					

Stander name (Chips name)	Module name	Actual FSB Speed	Advertised FSB Speed (2x) Data Rate (MHz)	Memory bus (64 bit)	Module Throughput (MBps)
DDR-400	PC-3200	200	400	8 bytes	3200 MBps

PC3200 is DDR SDRAM designed to operate at 200 MHz using DDR-400 chips with a bandwidth of 3,200 MB/s.
As the memory is double pumped, this means that the effective clock rate of PC3200 memory is 400 MHz

Double data Rate 2 (DDR2) SDRAM

- is like an evolution from the DDR SDRAM
- DDR2 was not meant to be a multiplier,
- but instead a revision mark of sorts.
- DDR2 achieve a total of 4 data transfers per memory clock

Stander name (Chips name)	Module name	Actual FSB Speed (MHz)	Advertised FSB Speed (4x)	Memory bus (64 bit)	Module Throughput (MBps)
DDR2-400	PC2-3200	100	400	8 bytes	**3200MBps**
DDR2-533	PC2-4200(4300)	133	533	8 bytes	**4266MBps**
DDR2-667	PC2-5300(5400)	166	667	8 bytes	**5333 MBps**
DDR2-800	PC2-6400	200	800	8 bytes	**6400 MBps**
DDR2-1066	PC2-	266	1066	8 bytes	8533

Module Throughput =FSB Speed (MHz)X Memory bus(bytes)

Double data Rate 3 (DDR) SDRAM

- is like an evolution from the DDR 2 SDRAM
- was designed to roughly double the performance of DDR2 products.
- *DDR3 is a memory type that was designed to be twice as fast as* the DDR2 memory that operates with the same FSB speed.
- 8 operations per cycle

Stander name (Chips name)	Module name	Actual FSB Speed (MHz)	Advertised FSB Speed (8x)	Memory bus (64 bit)	Module Throughput (MBps)
DDR3-800	PC3-6400	100	800	8 bytes	**6400MBps**
DDR3-1066	PC3-8500	133	1066	8 bytes	**8533MBps**
DDR3-1333	PC3-10600	166	1333	8 bytes	**10667**
DDR3-1600	PC3-12800	200	1600	8 bytes	**12800**

Module Throughput =FSB Speed (MHz)X Memory bus(bytes)

Direct Rambus DRAM (DRDRAM) or (RDRAM)

- Its memory design found in high-end PC systems from late 1999 through 2002.
- Intel signed a contract with Rambus (the company that designed it) in 1996 ensuring it would support RDRAM into 2001.
- After 2001, Intel continued to support RDRAM in existing systems, but new chipsets and motherboards primarily shifted to DDR SDRAM, and all future Intel chipsets and motherboards are being designed for either conventional DDR or the newer DDR2 standard.
- is a proprietary SDRAM technology
- Increased latency, heat output, complexity in the manufacturing process, and cost are the primary shortcomings

Stander name (Chips name)	Module name	Actual FSB Speed	Advertised FSB Speed (2x) Data Rate	Memory bus (64 bit)	Module Throughput (MBps)
RIMM 1200	PC-600	300	600	2 bytes	**1200**
RIMM1400	PC-700	350	700	2 bytes	**1400**
RIMM1600	PC-800	400	800	2 bytes	**1600**
RIMM2001	PC-1066	533	1066	2 bytes	**2133**
RIMM2004	PC-1200	600	1200	2 bytes	**2400**
RIMM3200	PC-800	400	800	4 bytes	**3200**
RIMM4200	PC-1066	533	1066	4 bytes	**4266**
RIMM4800	PC-1200	600	1200	4 bytes	**4800**

Module Throughput =FSB Speed (MHz)X Memory bus(bytes)

Memory Packaging

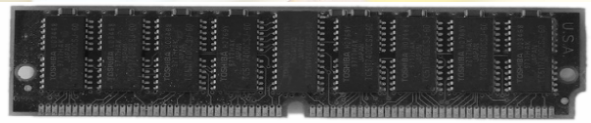
1. Single Inline Memory Modules
2. DIMM
3. RIMM
4. SODIMM
5. MicroDIMM

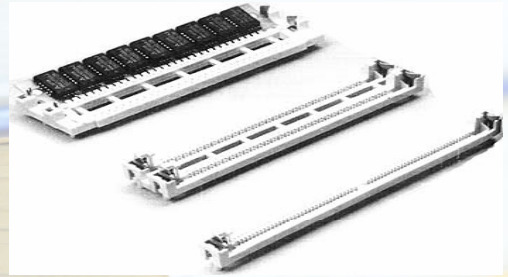
1- Single Inline Memory Modules

- in older computer systems.
- ***There are two types of SIMMs:***

1. The 30-pin units, which were introduced first, transfer data 8 bits at a time.

2. The 72-pin SIMMs transfer data 32 bits at a ti

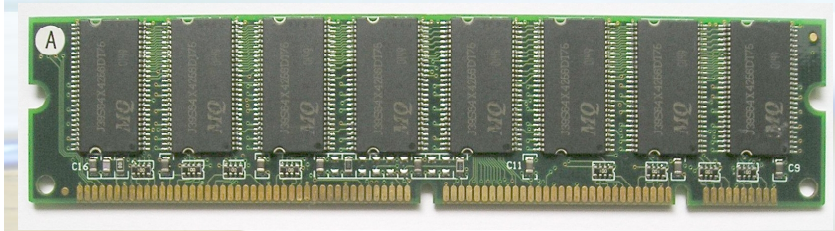




2-Dual Inline Memory Modules DIMMs

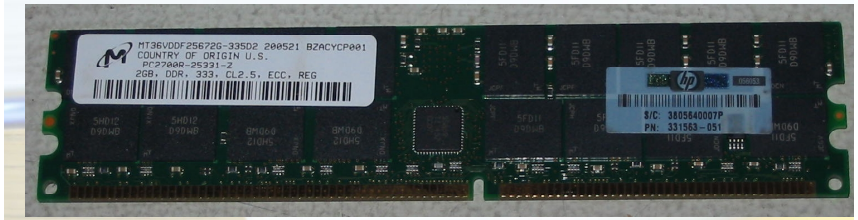
- Most common type of PC memory in use today
- DIMMs are 64-bit memory modules that are used as a package for the SDRAM family: SDR, DDR, DDR2, and DDR3.
- The term *dual* refers to the fact that, unlike their SIMM predecessors, DIMMs differentiate the functionality of the pins on one side of the module from the corresponding pins on the other side.

An SDR dual inline memory module (DIMM)



With 84 pins per side,
This makes 168 independent pins on each standard SDR module, as
shown with its two keying notches as well as the last pin labeled 84 on the side shown in

Double data rate (DDR) SDRAM

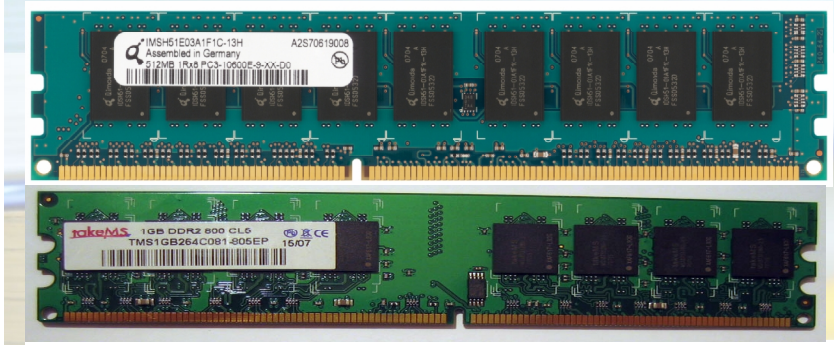


The DIMM used for DDR memory has a total of 184 pins and a single keying notch,

Double data rate (DDR2) SDRAM

while the DIMM used for DDR2 has a total of
240 pins,
one keying notch,
and possibly an aluminum cover for both sides, called a *heat spreader*, designed like a heat sink to dissipate
heat away from the memory chips and prevent overheating.

Double data rate (DDR3) SDRAM

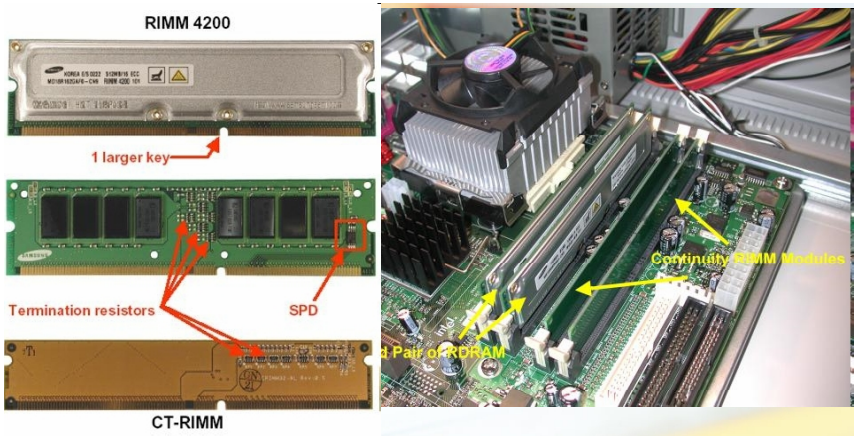


The DDR3 DIMM is similar to that of DDR2.
It has 240 pins and a single keying notch, but the notch is in a different location to avoid cross-insertion.
Not only is the DDR3 DIMM physically incompatible with DDR2 DIMM slots, it's also electrically incompatible.

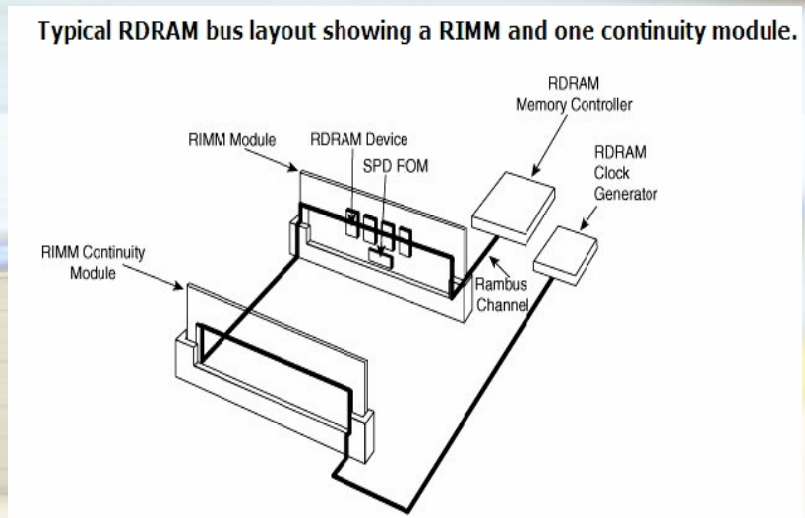
RIMM

The 16-bit modules have 184 pins and two keying notches must be filled in pairs

32-bit modules have 232 pins and only one keying notch, requires only a single motherboard slot

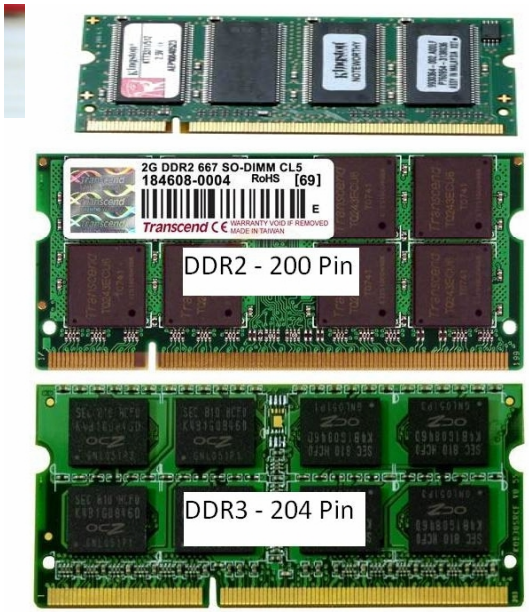


Continuity RIMM (CT-RIMM)
Since there cannot be any unused RIMM slots on a motherboard, a C-RIMM is a special module used to fill any unused RIMM slots. It is basically a RIMM module without any memory chips.



3-Small Outline DIMM SODIMM

- are a smaller alternative to a DIMM, being roughly half the size of regular DIMMs.
- SO-DIMMS are often used in systems which have space restrictions such as notebooks, small footprint PCs ,high-end upgradeable office printers, and networking hardware like routers.
- SO-DIMMs have 72, 100, 144, 200 or 204 pins.
- The 72 and 100 pin packages supports 32-bit data transfer,
- while the 144, 200 and 204 pin packages support 64-bit data transfer.
- This compares to regular DIMMs that have 168, 184, or 240 pins, all supporting 64-bit data transfer.[
- Most types of SO-DIMMs can be recognized at a glance by the distinctive notches used to "key" them for different applications:
- 100-pin SO-DIMMs have two notches,
- 144-pin SO-DIMMs have a single notch near (but not at) the center,
- and 200-pin SO-DIMMs have a single notch nearer to one side.



MicroDIMM

- The MicroDIMM is an extremely small RAM form factor.
- 50 percent smaller than a SODIMM,
- only 45.5 millimeters (about 1.75 inches) long and 30 millimeters wide.
- It was designed for the ultralight and portable subnotebook style of computer.
- These modules have 144 pins or 172 pins and are similar to a DIMM in that they use a 64-bit data bus.

MEMORY BANKS AND BANK SCHEMAS

memory bank is the number of memory slots needed to fill the data path of the processor.